Primeiro Desafio

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**VHDL**

library IEEE;

use IEEE.std\_logic\_1164.all;

entity latch\_d is

port (

D1, D2 : in bit;

ENB : in bit;

Q1, Q2 : out bit

);

end latch\_d;

architecture nv\_logic of latch\_d is

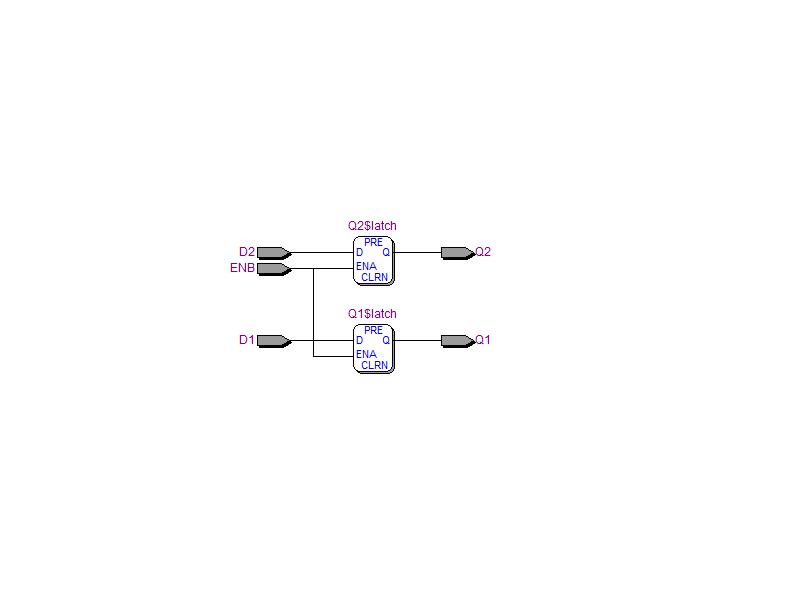
begin

Q1 <= D1 when ENB='1';

Q2 <= D2 when ENB='1';

end nv\_logic;

**RPL**



**Sim waveform**

